55. The USB host system of Claim 49, wherein the communication area includes a third area with a third pre-defined format to report device connection and/or removal from the main processor.

56. The USB host system of Claim 49, wherein the communication area includes a fourth area for storing a USB command in a fourth pre-defined format for sending a USB command to the processor.

57. The USB host system of Claim 49, wherein the starting address of the communication areas are used to identify a transfer.

58. The USB host system of Claim 49, wherein the main processor may allocate the dual port memory areas for a transfer.

59. The USB host system of Claim 51, wherein the dual port memory may implement isochronous, interrupt and/or bulk transfers.

REMARKS

These remarks are in response to the Office Action dated July 2, 2002 which has a statutory period for response ending October 2, 2002. The Examiner rejected the title of the invention. The Examiner also rejected Claims 1-16 under U.S. Patent No. 6,393,493 (Madden et al.) under 35 U.S.C. §102 and Claims 17-48 as being anticipated by U.S. Patent No. 6,009,480 (Pleso et. al). The Examiner also rejected Claim 4, 7, and 8 under 35 U.S.C. § 112 for insufficient antecedent basis. The Examiner objected to Claims 10 and 46. Applicants have amended Claims 1, 5, 7, 9, 10, 11, 24 and 46, and added Claims 49-59 to further clarify the invention and any change of scope is merely incidental. Applicants have also added a new title of the invention. Claims 1-59 are now pending in the above-identified application, of which Claims 1, 11, 17, 24, 41 and 49 are independent Claims. Reconsideration and allowance are respectfully requested in view of the amendments and the following remarks.

Title

The Examiner had rejected the title of the invention as not being descriptive. Applicants have replaced the title of the invention with "SYSTEM FOR TRANSFERING DATA USING A USB HOST SYSTEM WITH A DEDICATED PROCESSOR" a title that is descriptive of the invention. Applicant respectfully request that this rejection be withdrawn.

Rejection under 35 U.S.C. § 112

In the Office Action (Page 2), the Examiner rejected Claims 4, 7 an 8 under 35 U.S.C. § 112 for lacking antecedent. Applicants have amended Claim 1 to add the term "main processor" and hence Claim 4 that depends from Claim 1 has the appropriate antecedent basis for the "main processor" limitation. Applicants have also amended Claim 7 to state "a USB bus" instead of "the USB bus", and hence have the proper antecedent basis for the limitation. Based on the Claim 7 amendment, Claim 8 also has the proper antecedent basis for "the USB bus" limitation.. Accordingly, Applicants respectfully request reconsideration and withdrawal of the above 35 U.S.C § 112 rejection.

Rejection under 35 U.S.C. § 102

CLAIM 1

The Examiner rejected claims 1-16 under 35 U.S.C. § 102(e) as being anticipated by Madden.

Madden fails to suggest or disclose the elements of Claim 49. In particular, Madden does not disclose a USB host system operationally coupled to a computing system with a main processor. Madden also fails to disclose or suggest a USB host system that includes a first processor that implements a function of a USB driver without using the main processor resources; a downstream USB port; and a communication area accessible both by the main processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in

the communication area in a pre-defined record format and the first processor schedules and completes the request via a USB host controller.

Madden discloses a USB based data acquisition system with a virtual buffer in main memory (Figure 1, 146). "The virtual buffer operates to receive or intercept calls made by the DAQ driver level software to acquire data from the device" [Madden, Abstract].

The draw backs of the system disclosed in Madden is what the present invention intends to solve. In Madden, the main CPU (Fig 1 , 140) runs the USB driver and the host controller driver. Contrary to Madden in the present invention, main processor 310 (Figure 3 of the application) does not run the USB and host controller driver. The USB host system of Claim 1 removes the burden on main processor 310 to manage or service USB transfers.

The Examiner has relied on various Madden components in the office action to reject Claims 1-16. More particularly, the Examiner states:

> "Madden substantially discloses a USB host system (fig 3, 206)" comprising: a first processor implementing a function of a USB driver. (fig 4, 226)(fig. 2, 180)(col. 5, lines 35-41)". (Office Action, Page 3)

Madden discloses a typical USB system. USB interface code 226 (Madden Fig. 4) interfaces with the DAQ driver level software 224 runs on CPU 140 with the operating system. [Madden, Col. 5, lines 14-21]. In Madden the USB driver and host controller driver are run on main CPU 140, a problem that the present invention solves.

In the present invention, the USB host system with its own processor (Fig. 2 item 210 of Applicants Specification) runs the USB driver and host controller driver. This removes the burden of managing and servicing USB devices from the main processor.

The Examiner further states:

"a communication area accessible both by a second processor and by the first processor"

Madden does not disclose "a communication area accessible both by the main processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the first processor schedules and completes the request via a USB host controller' [Claim 1]

The Exminer has cited "main memory 146" of Madden against the communication area of Claim 1. Madden's main memory 146 does not show that "the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats".

For the foregoing reasons, Applicants invention as stated in the amended Claim 1 is not disclosed by Madden. Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 1 under 35 U.S.C. § 102(e).

CLAIMS 2-10

Claims 2-10 depend on Claim 1 and are thus patentable over Madden for at least the same reasons provided above with respect to amended Claim 1. Accordingly, withdrawal of Examiner's rejection of Claims 2-10 is respectfully requested.

CLAIM 11

Madden does not disclose the elements of amended Claim 11 for at least the same reasons as set forth above with respect to Claim 1. Accordingly, withdrawal of Examiner's rejection of Claims 11 is respectfully requested.

CLAIM 12-16

Claims 12-16 depend on Claim 11 and are thus patentable over Madden for at least the same reasons provided above with respect to amended Claims 1 and 11. Accordingly, withdrawal of Examiner's rejection of Claims 12-16 is respectfully requested.

CLAIM 17

The Examiner rejected Claims 17-48 as being anticipated by Pleso.

Pleso fails to disclose the elements of Claim 17. In particular, Pleso fails to disclose a "second processor implementing a first data transfer driver managing a data transfer between the said first processor and a device; and an interface with the first processor that provides a high-level view of the data transfer process to the first processor" [Claim 17].

Pleso discloses "a method and system for providing and installing a device driver, and more particularly to a system of integrating a device driver with the device itself." [Pleso, Col. 2, Lines 39-42]. Pleso also discloses "a method for retrieving the device driver software from the peripheral device upon powering of the computer system". [Pleso, Col. 2, lines 46-48].

Unlike Pleso, the present invention is not about retrieving a device driver from a device, as disclosed by Pleso.

The Examiner compares the first processor 310 (Fig. 3) and the second processor (Fig. 2, 210) of Claim 17 of the present invention with the single "processor 20" of Pleso [Pleso, Fig.1]. Unlike Pleso where processor 20 (Pleso, Fig. 1) conducts most of the operations, in the present invention, two separate processors are used and the USB driver functionality is moved from the main processor to the USB system processor.

For the foregoing reasons, Applicants invention as stated in the Claim 17 is not disclosed or anticipated by Pleso. Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 17 under 35 U.S.C. § 102(e).

CLAIMS 18- 23

Claims 18-23 depend on Claim 17 and are thus patentable over Pleso for at least the same reasons provided above with respect to Claim 17. Accordingly, withdrawal of Examiner's rejection of Claims 18-23 is respectfully requested.

CLAIM 24

Madden does not disclose the elements of Claim 24 for at least the same reasons as set forth above with respect to Claim 17. Accordingly, withdrawal of Examiner's rejection of Claims 24 is respectfully requested.

CLAIMS 25-40

Claims 25-40 depend on Claim 24 and are thus patentable over Pleso for at least the same reasons provided above with respect to Claim 17 and 24. Accordingly, withdrawal of Examiner's rejection of Claims 25-40 is respectfully requested.

CLAIM 41

Madden does not disclose the elements of Claim 41 for at least the same reasons as set forth above with respect to Claim 17 and 41. Accordingly, withdrawal of Examiner's rejection of Claims 41 is respectfully requested.

CLAIM 41-48

Claims 41-48 depend on Claim 40 and are thus patentable over Pleso for at least the same reasons provided above with respect to Claim 17. Accordingly, withdrawal of Examiner's rejection of Claims 25-40 is respectfully requested.

NEW CLAIMS 49-59

Madden and Pleso do not disclose the elements of Claim 49-59 for at least the same reasons as set forth above with respect to Claims 1 and 17. Accordingly, Claim 49-59 are believed to be allowable.

CONCLUSION

For the foregoing reasons, Applicant believes Claims 1-59 are allowable, and a notice of allowance is respectfully requested. If the Examiner has any questions regarding the application, the Examiner is invited to call the undersigned Attorney at (949) 955-1920.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on **October 1, 2002**.

10/1/2002

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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Attorney for Applicants
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the following paragraph, deletions are shown in brackets and additions are underlined.

TITLE of the Invention:

[USB HOST SYSTEM]

"SYSTEM FOR TRANSFERING DATA USING A USB HOST SYSTEM WITH A DEDICATED PROCESSOR"

IN THE CLAIMS

1. A USB host system operationally coupled to a computing system with a main processor, comprising:

a first processor that implements [implementing a function of] a USB driver without using the main processor resources;

a downstream USB port;

a communication area accessible both by the main [second] processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the first processor schedules and completes the request via a USB host controller.

5. The USB host system of [in] Claim 1 where the [said] main processor interfaces the host system via a standard microprocessor bus.

7. The USB host system of [in] Claim 1 where data in the communication area is [are] directly sent out on a [the]USB bus.

9. The USB host system of [in] Claim 1 where the [said] USB host system provides a USB function to the [said] main [second] processor.

10. The USB host system of [in] Claim 1 where the [said]USB host system is used to provide a USB host function to the said second processor which runs an operating system supporting USB , by intercepting call to a USB driver [USBD] in the [said] operating system.

11. A USB host system operationally coupled to a computing system, comprising:

a first processor implementing a function for managing a USB host controller with or without an operating system running on the computing system;

a down stream USB port;

an interface between the first processor and a second processor that provides a high-level USB pipe view of a USB system to an application [a] program running on the [a] second processor in the computing system.

24. A USB host comprising:

a first processor implementing a function of a USB system;

a downstream USB port; and

a memory accessible by [both] the [said] first processor and a [an] second processor external to the [said] USB host, where a first area of the memory with first predetermined format is used for a first type of transfer, and a second area of the memory with a second predetermined format is used for a second type of transfer.

46. The USB host of [in] Claim 41 where the second processor runs an operating system that supports USB and USB transfer request by the said second processor to USB driver [USBD] on the second processor on the second processor is carried out by the [said] USB host.

49. A USB host system operationally coupled to a computing system with a main processor, comprising:

a processor that interfaces with the main processor via a communication area using predefined records in pre-defined formats, wherein the main processor writes a data

transfer request in the communication area in a pre-defined record format and the processor schedules and completes the request via a USB host controller.

50. The USB host system of Claim 49, wherein the processor returns status and data to the main processor based on a request from the main processor.

51. The USB host system of Claim 49, wherein the communication area is a dual port memory with plural registers.

52. The USB host system of Claim 49, wherein the main processor may poll the communication area and/or be notified by an interrupt generated by the processor.

53. The USB system of Claim 49, wherein the communication area is divided into a first area with a predefined format for a first type of transfer, and a second area with a second pre-defined format for a second type of transfer.

54. The USB host system of Claim 49, wherein the main processor and the processor are operationally coupled via a standard microprocessor bus interface.

55. The USB host system of Claim 49, wherein the communication area includes a third area with a third pre-defined format to report device connection and/or removal from the main processor.

56. The USB host system of Claim 49, wherein the communication area includes a fourth area for storing a USB command in a fourth pre-defined format for sending a USB command to the processor.

57. The USB host system of Claim 49, wherein the starting address of the communication areas are used to identify a transfer.

58. The USB host system of Claim 49, wherein the main processor may allocate the dual port memory areas for a transfer.

59. The USB host system of Claim 51, wherein the dual port memory may implement isochronous, interrupt and/or bulk transfers.